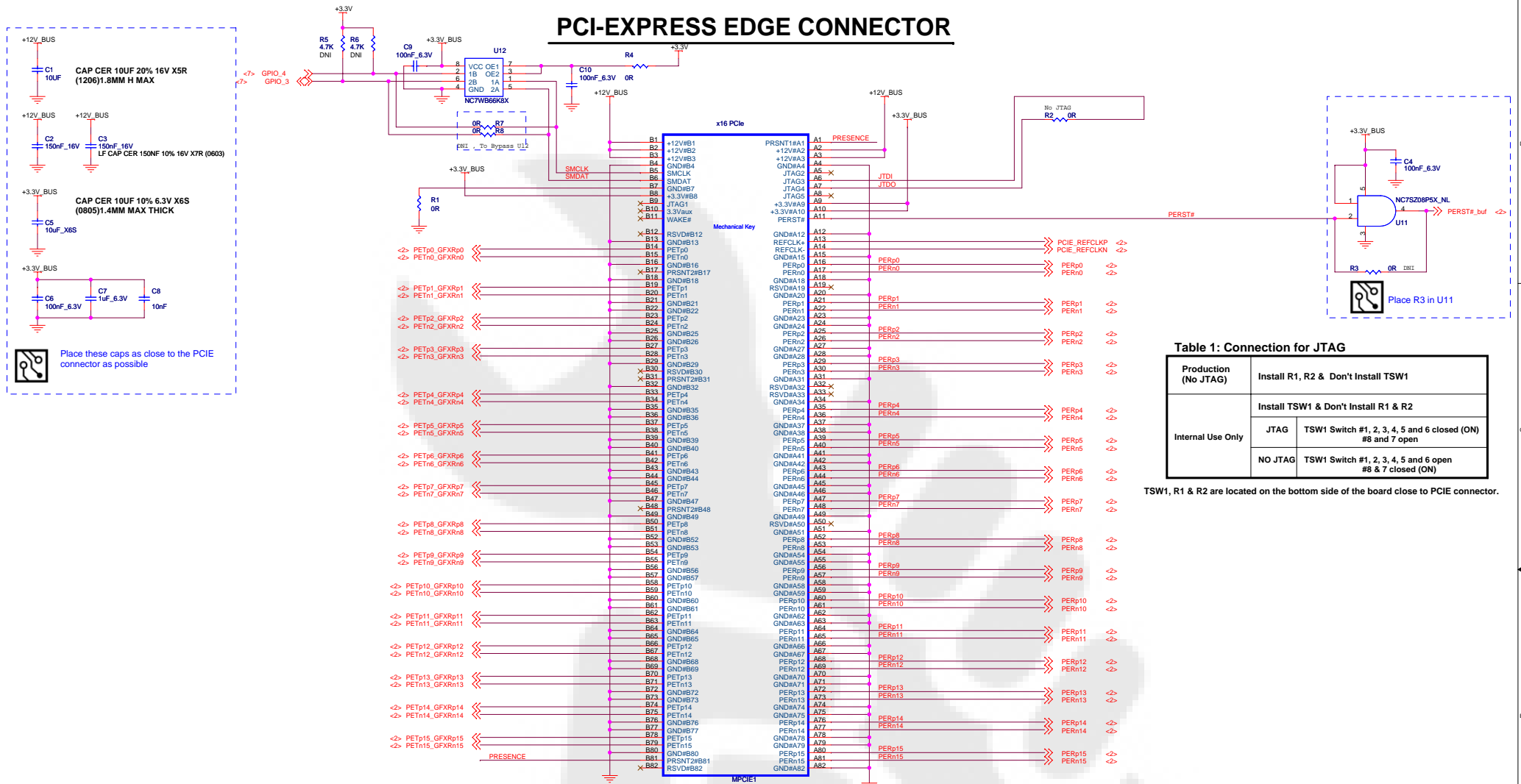


# PCI-EXPRESS EDGE CONNECTOR

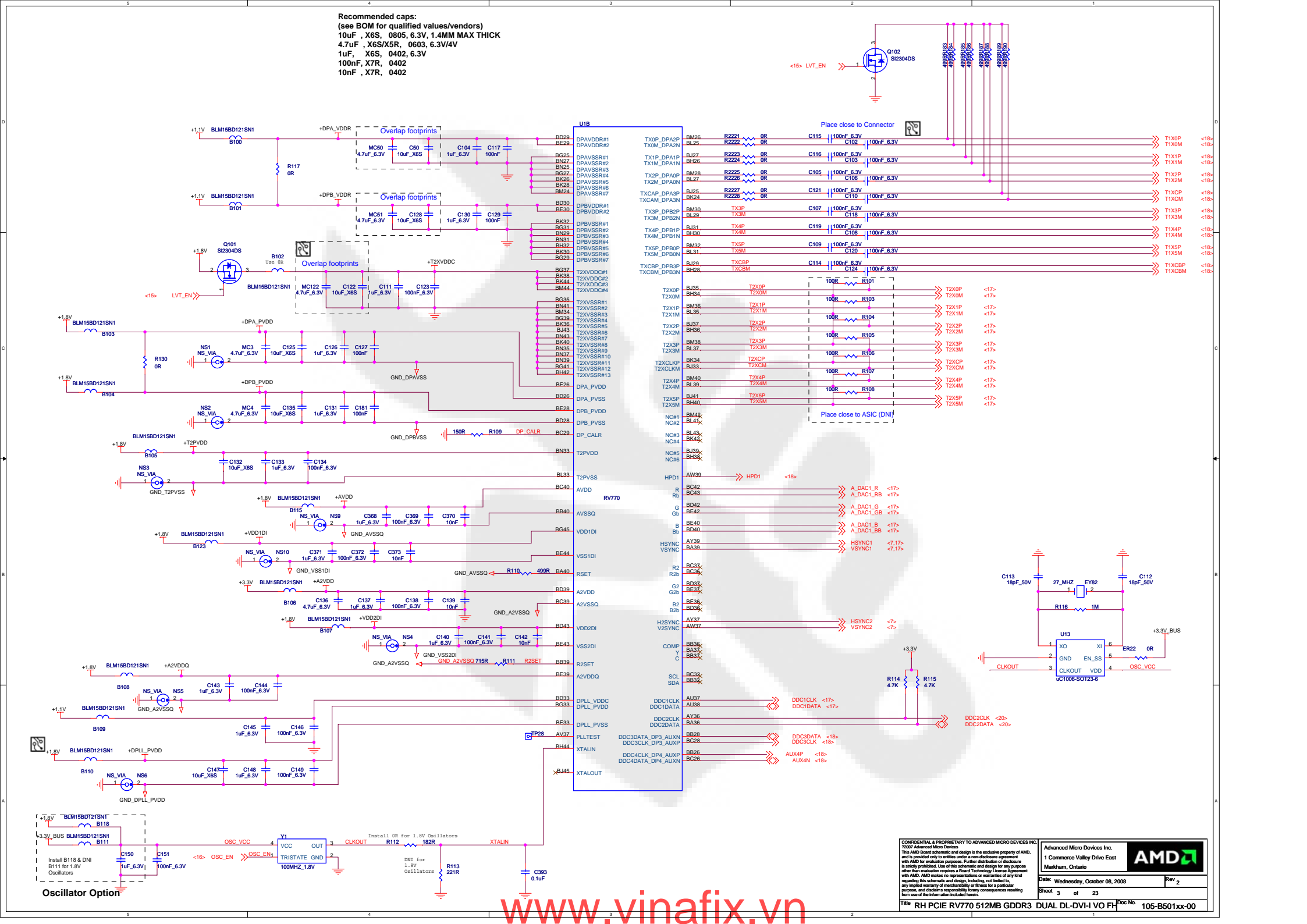


TSW1, R1 & R2 are located on the bottom side of the board close to PCIe connector.

SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
BUO	BRING UP ONLY



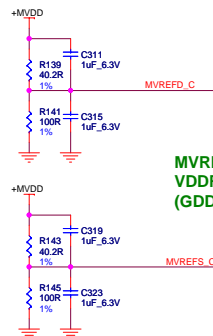
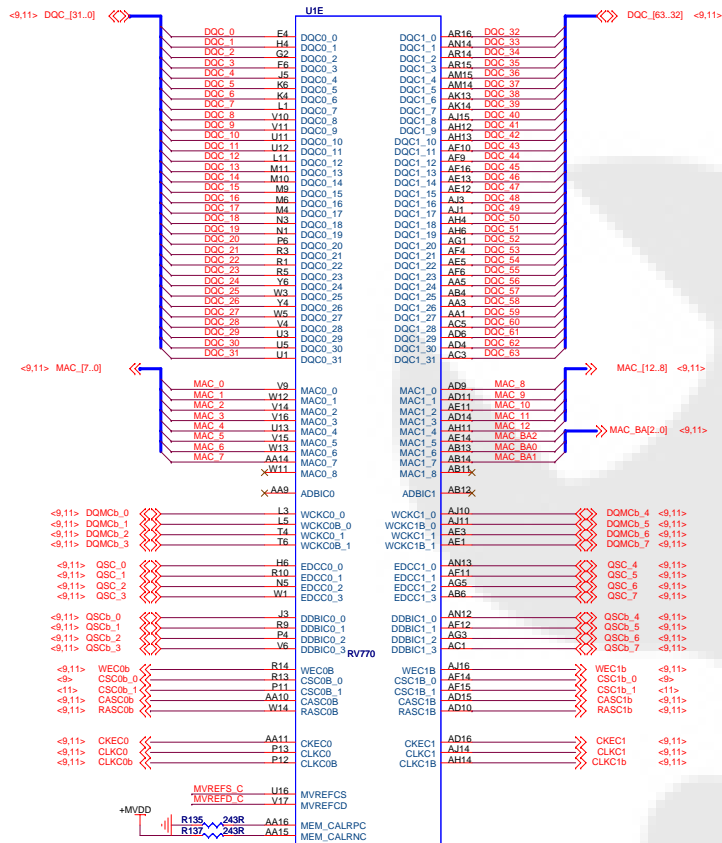
Recommended components  
(see BOM for qualified values/vendors)  
10uF , X6S, 0805, 6.3V, 1.4MM MAX THICK  
4.7uF , X6S/X5R, 0603, 6.3V/4V  
1uF , X6S, 0402, 6.3V  
100nF, X7R, 0402  
10nF , X7R, 0402



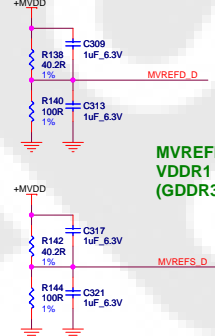
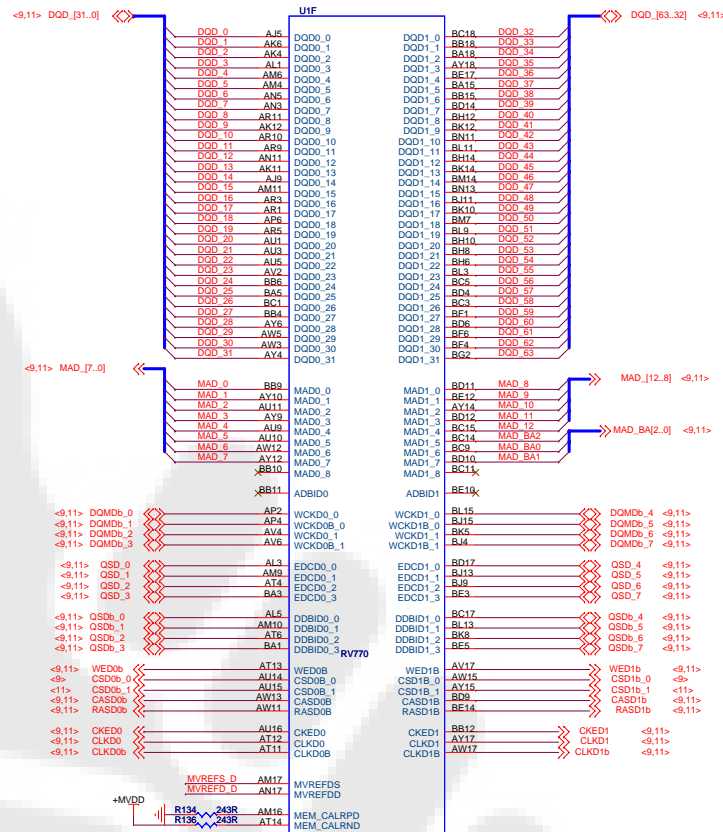








MVREFD/S = 0.7\*  
VDDR1  
(GDDR3/4/5)

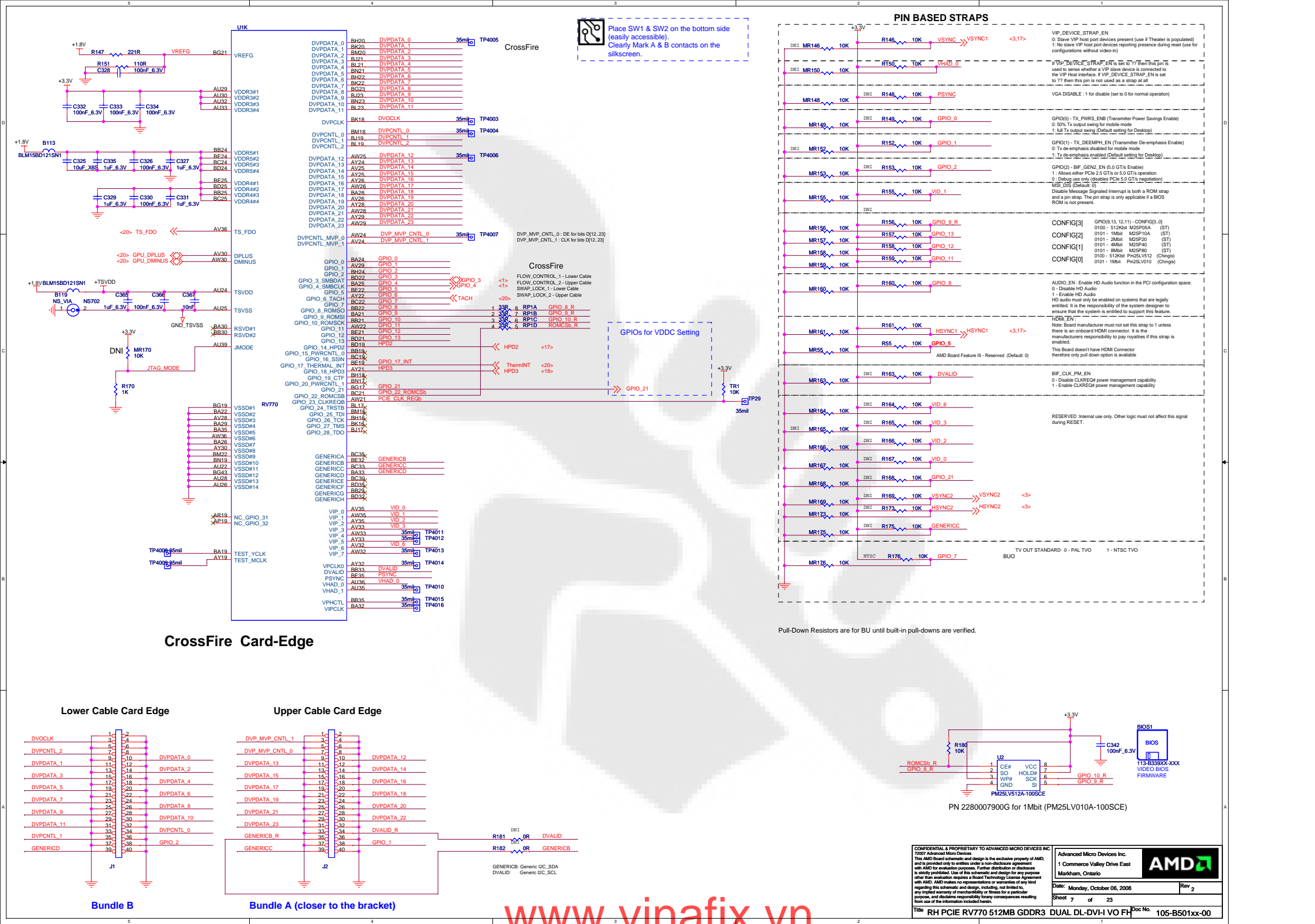


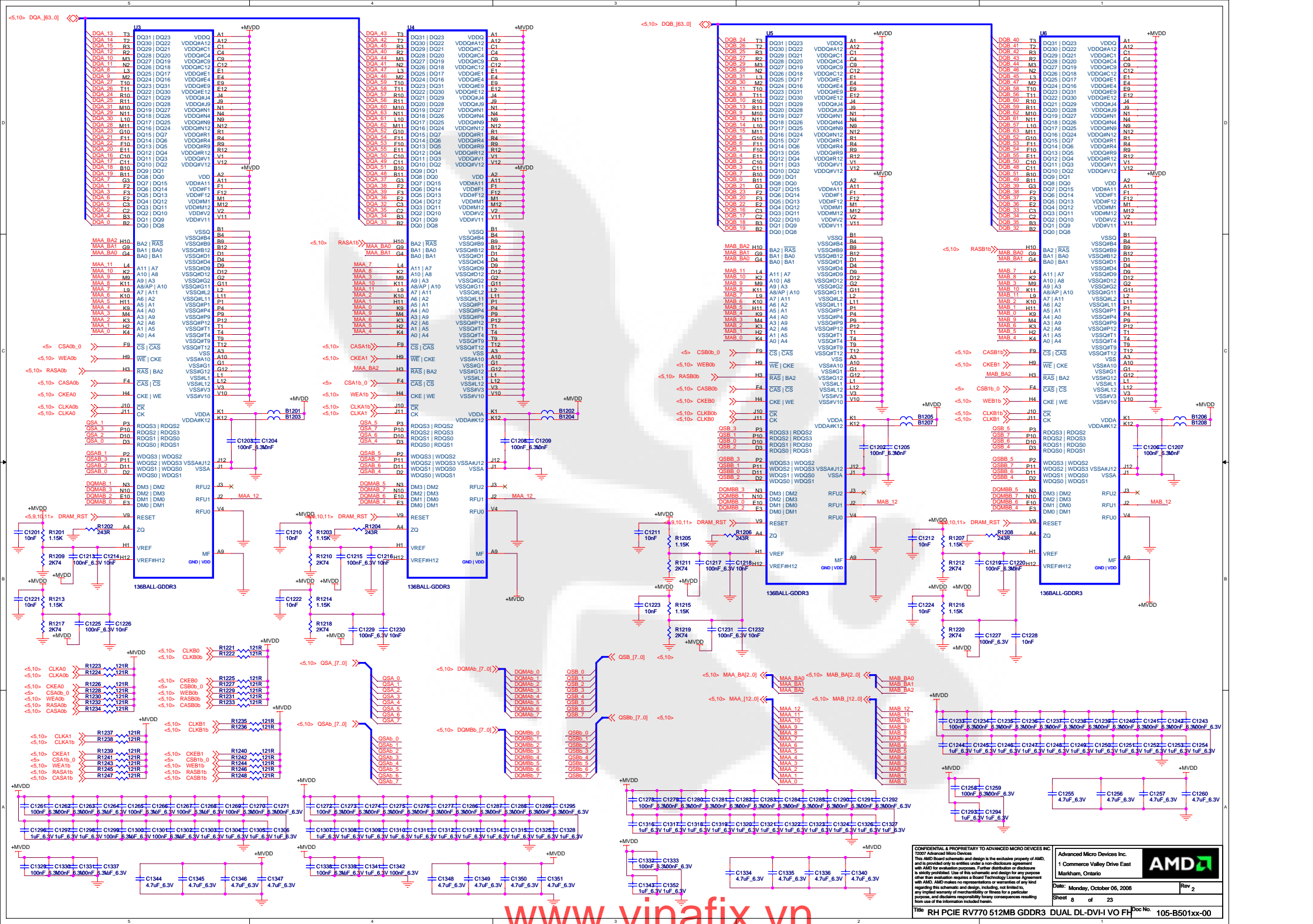
MVREFD/S = 0.7\*  
VDDR1  
(GDDR3/4/5)

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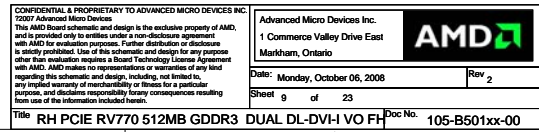
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1 Commerce Valley Drive East  
Markham, Ontario  
Date: Monday, October 06, 2008  
Sheet 6 of 23  
Rev 2

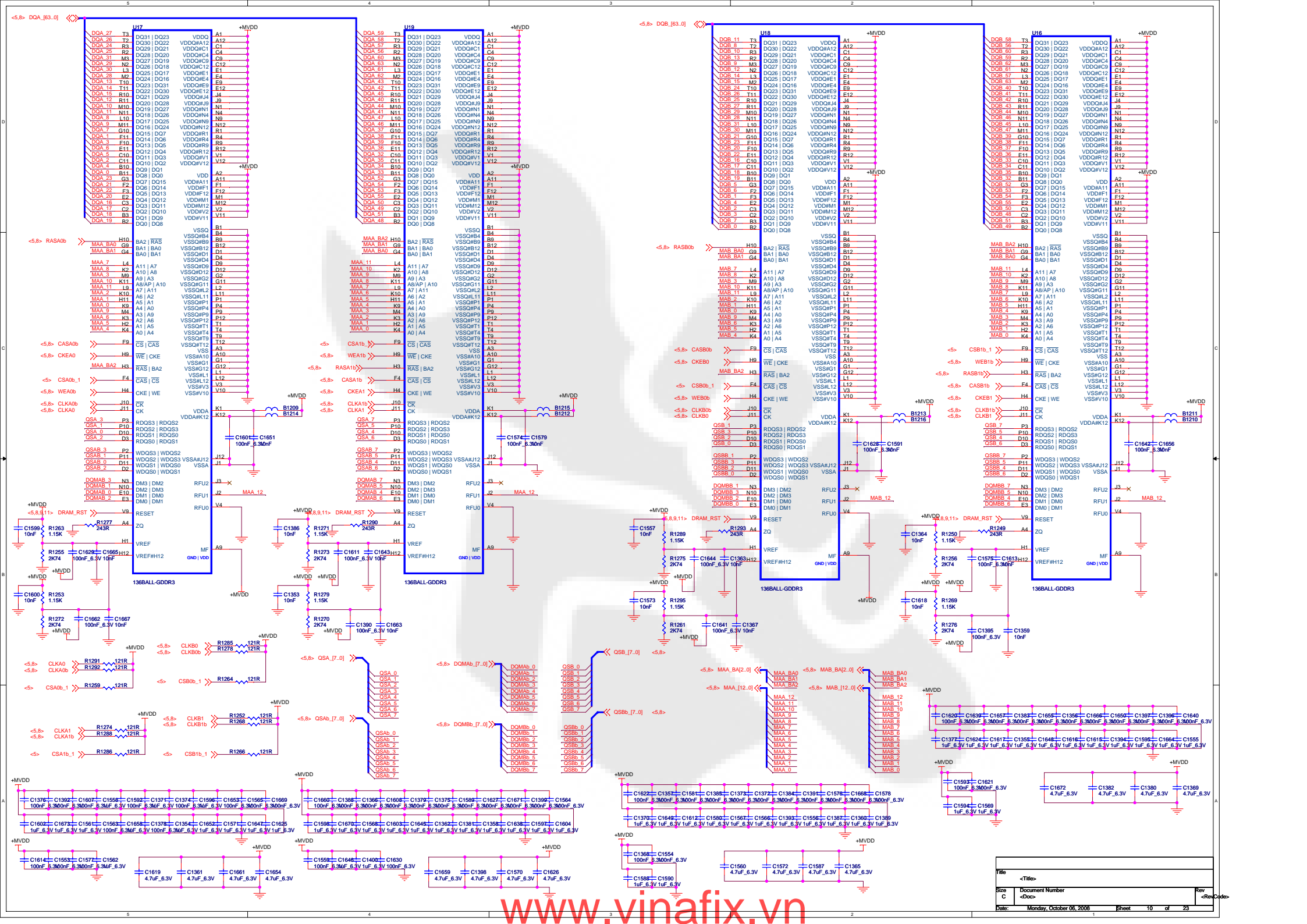














Title			
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Size C	Document Number		Rev
	<Doc>		<Rev>
Date:	Monday, October 06, 2008		Sheet 11 of 23



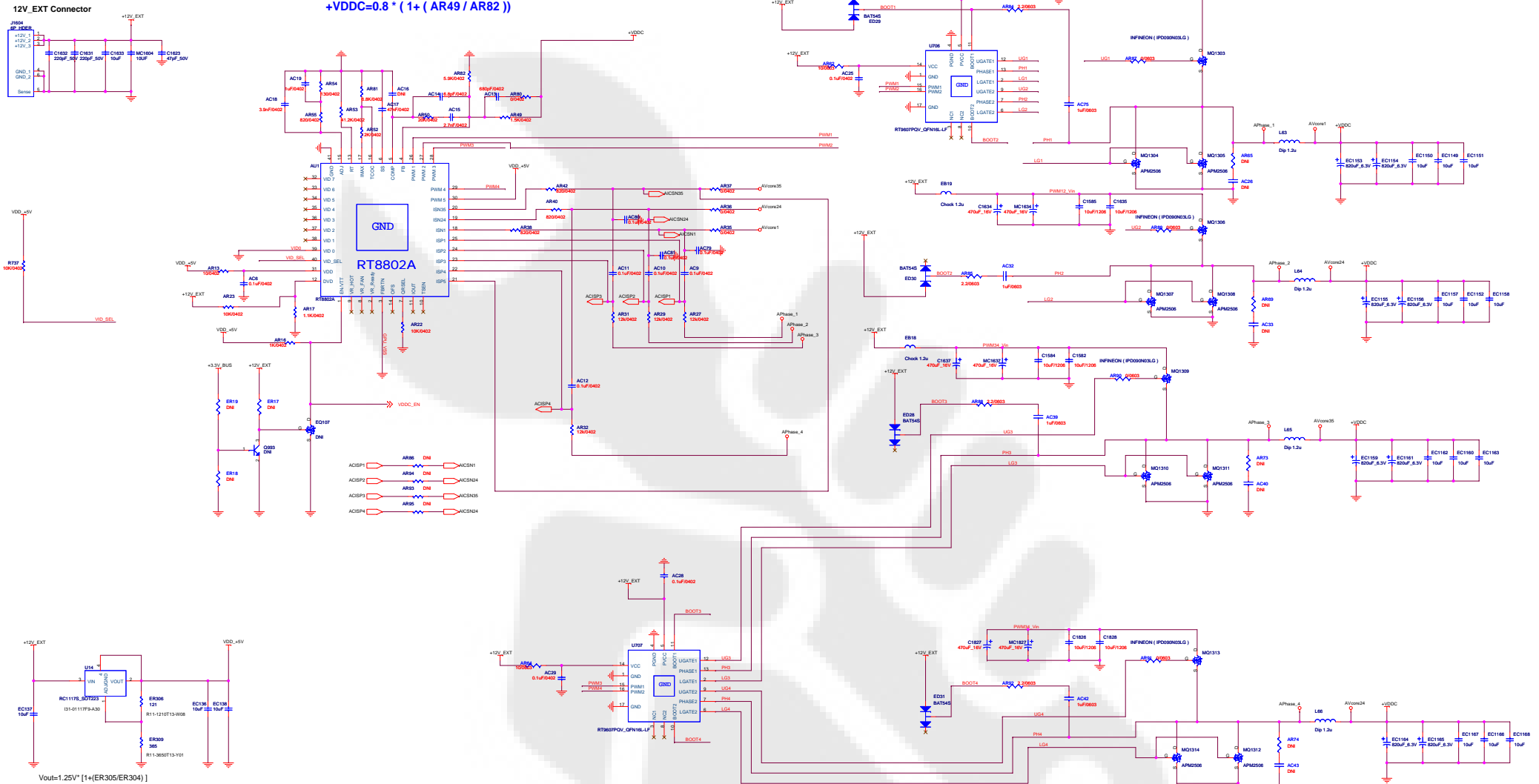
U1J

<del>BK49</del>	SP_RX0P	SP_TX0P	<del>BH48</del>
<del>BL51</del>	SP_RX0N	SP_TX0N	<del>BH49</del>
<del>BJ50</del>	SP_RX1P	SP_TX1P	<del>BC45</del>
<del>BG52</del>	SP_RX1N	SP_TX1N	<del>BC44</del>
<del>BE48</del>	SP_RX2P	SP_TX2P	<del>BB45</del>
<del>BE49</del>	SP_RX2N	SP_TX2N	<del>BB44</del>
<del>BE51</del>	SP_RX3P	SP_TX3P	<del>AY42</del>
<del>BDS2</del>	SP_RX3N	SP_TX3N	<del>AY41</del>
<del>BD48</del>	SP_RX4P	SP_TX4P	<del>AY45</del>
<del>BC49</del>	SP_RX4N	SP_TX4N	<del>AY44</del>
<del>BC51</del>	SP_RX5P	SP_TX5P	<del>AW42</del>
<del>BDS2</del>	SP_RX5N	SP_TX5N	<del>AW41</del>
<del>BB48</del>	SP_RX6P	SP_TX6P	<del>AW45</del>
<del>BA49</del>	SP_RX6N	SP_TX6N	<del>AW44</del>
<del>BA51</del>	SP_RX7P	SP_TX7P	<del>AL42</del>
<del>AY52</del>	SP_RX7N	SP_TX7N	<del>AL41</del>
<del>AY48</del>	SP_RX8P	SP_TX8P	<del>AL45</del>
<del>AV49</del>	SP_RX8N	SP_TX8N	<del>AL44</del>
<del>AV51</del>	SP_RX9P	SP_TX9P	<del>AT42</del>
<del>AV52</del>	SP_RX9N	SP_TX9N	<del>AT41</del>
<del>AV48</del>	SP_RX10P	SP_TX10P	<del>AT45</del>
<del>AL49</del>	SP_RX10N	SP_TX10N	<del>AT44</del>
<del>AL51</del>	SP_RX11P	SP_TX11P	<del>AR42</del>
<del>AT52</del>	SP_RX11N	SP_TX11N	<del>AR41</del>
<del>AT48</del>	SP_RX12P	SP_TX12P	<del>AR45</del>
<del>AR49</del>	SP_RX12N	SP_TX12N	<del>AR44</del>
<del>AR51</del>	SP_RX13P	SP_TX13P	<del>AM42</del>
<del>AP52</del>	SP_RX13N	SP_TX13N	<del>AM41</del>
<del>AP48</del>	SP_RX14P	SP_TX14P	<del>AN45</del>
<del>AN49</del>	SP_RX14N	SP_TX14N	<del>AN44</del>
<del>AN51</del>	SP_RX15P	SP_TX15P	<del>AM42</del>
<del>AM52</del>	SP_RX15N	SP_TX15N	<del>AM41</del>
<del>BM47</del>	SP_REFCLKP	SP_CALRP	<del>AH39</del>
<del>BK46</del>	SP_REFCLKN	SP_CALRN	<del>AH38</del>

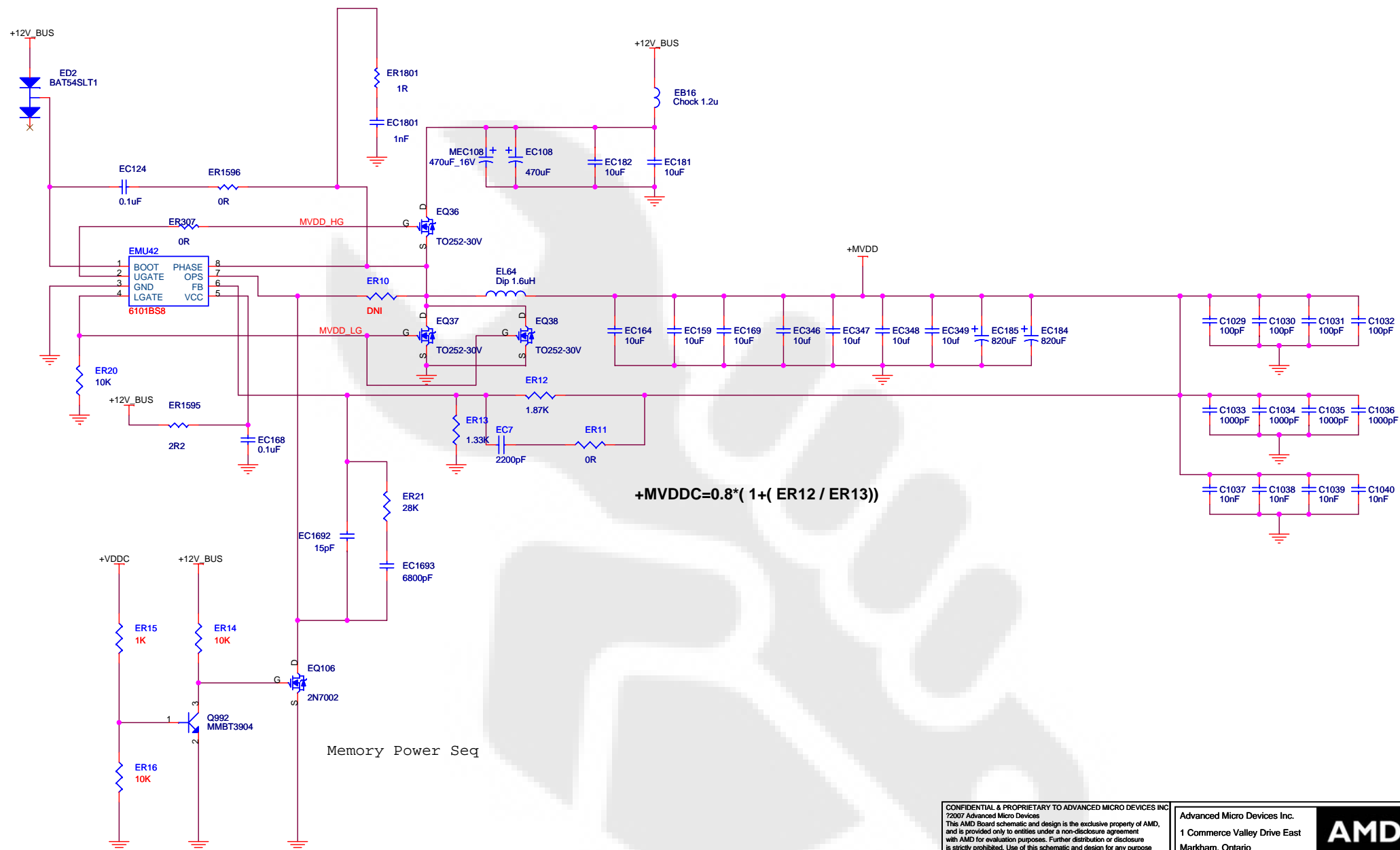
RV770

### Install AR47 for Disable PWM3 function

$$+VDDC=0.8 * ( 1+ ( AR49 / AR82 ) )$$


$$V_{out} = 1.25V * [1 + (R_{305}/R_{304})]$$





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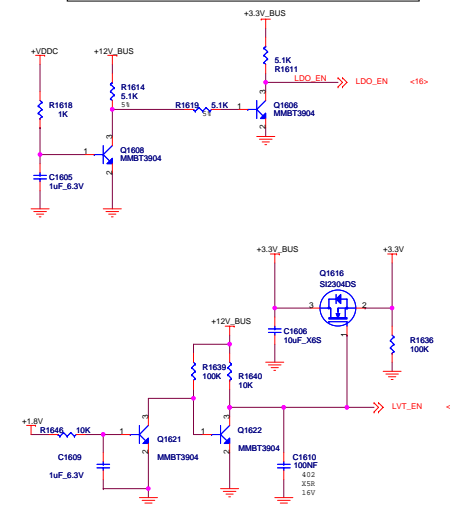
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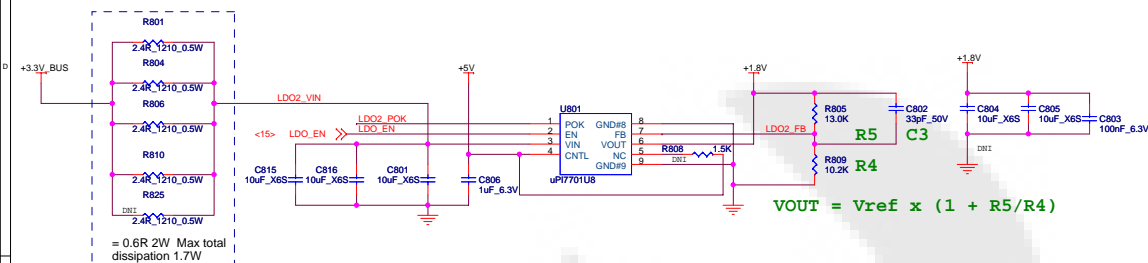
Date: Monday, October 06, 2008 Rev 2  
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Title RH PCIe RV770 512MB GDDR3 DUAL DL-DVI-I VO F Doc No. 105-B501xx-00

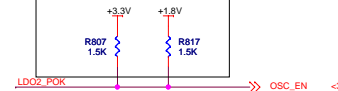
# Power up Sequencing



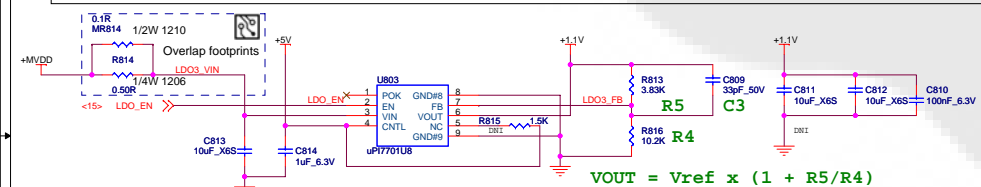
**LDO #2:** Vin = 2.5V to 3.6V MAX      Vout = +1.8V +/- 3%      Iout = 1.7A (TBV) RMS MAX  
PCB: Min 70mm sq. copper area for cooling



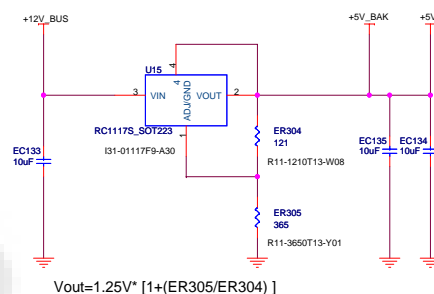
Install R817 if Y1 is a 1.8V Device  
Install R807 if Y1 is a 3.3V Device



**LDO #3: Vin = +1.50V to 2.1VMAX      Vout = +1.1V +/- 3%      Iout = Up to 1.3A (TBV) RMS MAX**  
**PCB: Min 70mm sq. copper area for cooling**



### Regulators for +5V, +5V\_VESA and +5V\_VESA2


$$V_{out} = 1.25V * [1 + (R_{305}/R_{304})]$$


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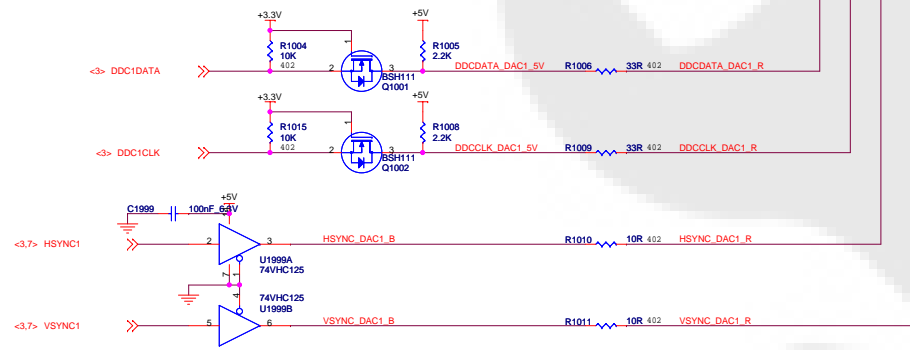
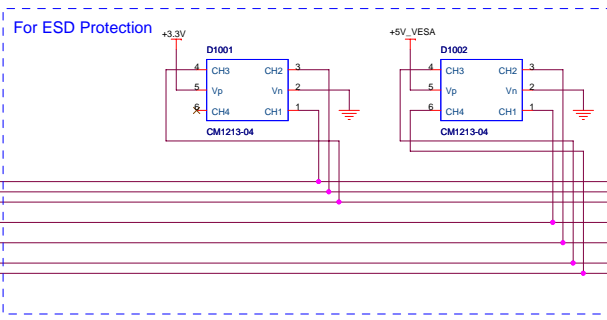
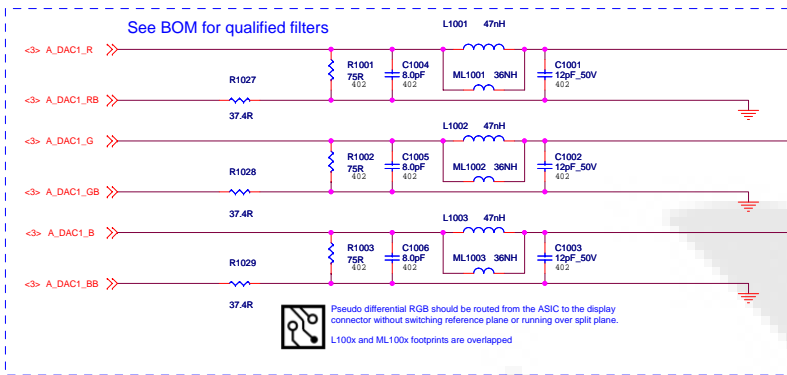
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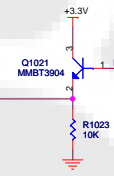


Date: Monday, October 06, 2008  
Sheet 16 of 23

Title	RH PCIE RV770 512MB GDDR3 DUAL DL-DVI-I VO F	Doc No.	105-B501xx-00
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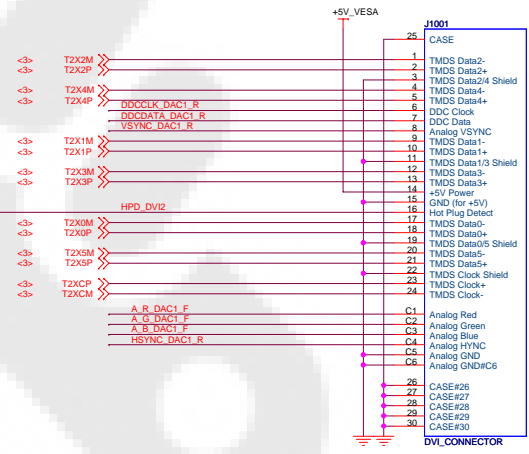


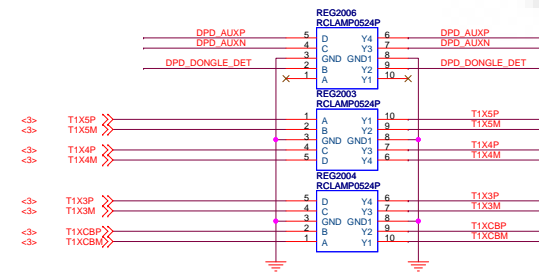
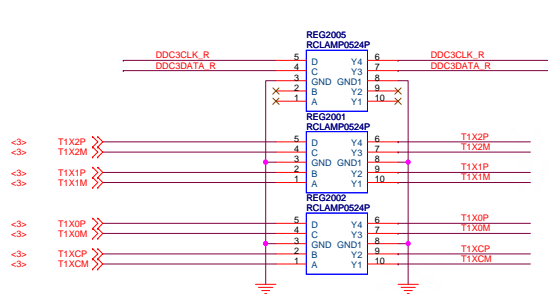
SYN and DDC should be routed from the ASIC to the display connector without switching reference plane or running over split plane



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Optional
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
15	Monitor ID bit 3	Open	Open	Open	Optional
9	N/C	+5V	+5V	+5V	Optional
Hardware Support	No	Yes	Yes	No	Yes

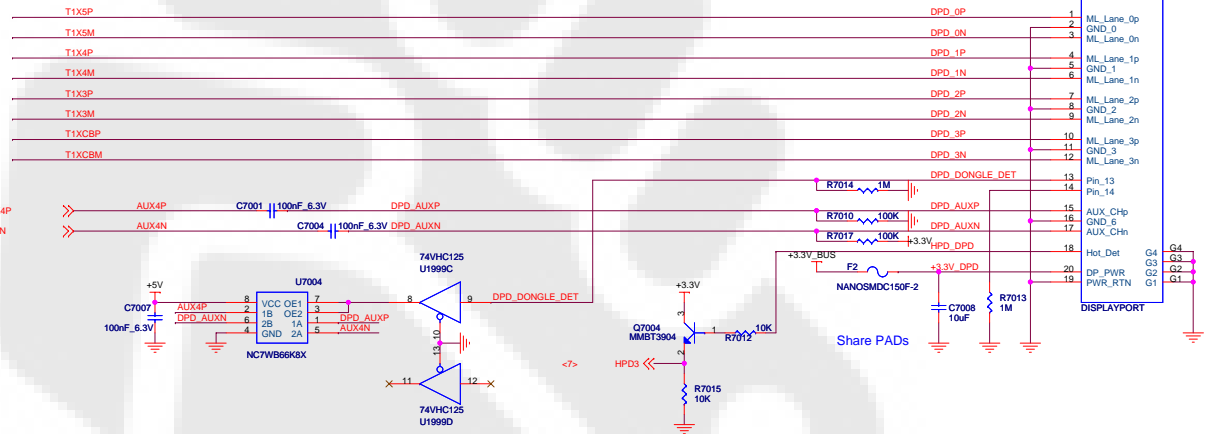
Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997





For ESD Protection  
Place  
Close to  
Connector

<> AUX4P  
<> AUX4N



DB15 pin	Standard VGA	DDC1 Host	DDC2B or DDC2B+ Host	DDC2AB Host	DDC1/2 Display
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional	
12	Monitor ID bit 1	Monitor ID bit 1	Monitor ID bit 1	Optional	
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional	
15	Monitor ID bit 3	Open	Open	Optional	
9	N/C	+5V	+5V	+5V	
	Mechanical Key	50mA min	50mA min	300mA min	
		1A max	1A max	1A max	
Hardware Support	No	Yes	Yes	No	Yes

Based on VESA Display Data Channel (DDC) Standard Ver. 3 Dec. 15, 1997

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Date: Wednesday, October 08, 2008

Rev 2

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Title: RH PCIe RV770 512MB GDDR3 DUAL DL-DVI-I VO FPC No. 105-B501xx-00

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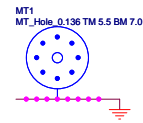
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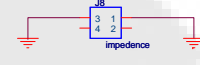
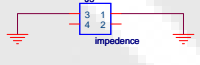
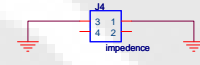
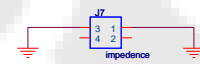
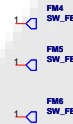
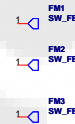
Date: Wednesday, September 24, 2008 Rev 2  
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Title RH PCIe RV770 512MB GDDR3 DUAL DL-DVI-I VO FH Doc No. 105-B501xx-00





## PCIE 12V/3.3V Power up Bonding support



<div>AMD</div>			Title		Schematic No.	Date:	
			RH PCIE RV770 512MB GDDR3 DUAL DL-DVI-I VO FH		105-B501xx-00	Tuesday, May 27, 2008	
			REVISION HISTORY				Rev 2
			NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.				
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION				
0	00A	07/10/11	Initial design for RV770 GDDR3				
1	00B	08/02/25	Improvement: 1) Add 1 uF CAP on memory reset, Pg5 2) MVDDC current leakage board workaround; Pg13 3) MVDD Thermal Protection, Pg 13 4) Improvement on Hot Plug protection Pg13 5) 12V_BUS & 12V_EXT Input Switch Circuit Page 13				
2	00	08/03/27	1. Correct PTC comparator power connection. 2. Add Fuse NF1200 on page 13				

